Docket No.: 49657-700

UTILITY PATENT APPLICATION UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Tsutomu YOSHIMURA, Harufusa KONDOH
FOR: A DIGITAL SYNCHRONOUS CIRCUIT FOR STABLY GENERATING OUTPUT CLOCK SYNCHRONIZED WITH INPUT DATA

Enclosed are:

- ☒ 27 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 11-347448
- ☒ 6 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	13	-20	0	$18.00	$0.00
Independent Claims	1	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$690.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$730.00

☒ Please charge my Deposit Account No. 500417 in the amount of $730.00. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417. A duplicate copy is enclosed.

- ☒ Any additional filing fees required under 37 CFR 1.16.

☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:klm
Date: June 1, 2000
Facsimile: (202) 756-8087

TITLE OF THE INVENTION

A Digital Synchronous Circuit for Stably Generating Output Clock Synchronized with Input Data

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a digital synchronous circuit for providing an output clock signal synchronized in phase with an input data signal from outside.

Description of the Background Art

One technique of implementing a synchronous circuit for providing an output clock signal synchronized with the phase of an input data signal sent serially from outside the chip is described in B. Kim, D. N. Helman, and P. Gray, "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2 μm CMOS," J. S. S. C. (Journal of Solid-State Circuits,) 1990 Vol. 25, No. 6, pp. 1385-1394.

In this technique, a method of generating and utilizing multiphase clock signals by voltage controlled oscillator (hereinafter referred to as VCO) formed by a group of inverters connected in a loop and whose delay time can be controlled is devised.

A multiphase clock generating circuit for generating the multiphase clock has a PLL (Phase Lock Loop) configuration in which the oscillation frequency of VCO is controlled to be the same as the frequency of an input data signal input from outside the chip. In this configuration, multiphase clock signals, i. e. a plurality of clock signals having the same frequency, a constant phase difference, and different phases, are output by taking out the signals from each node of the group of inverters connected in a loop within VCO.

Fig. 8 is a block diagram of the configuration of a conventional digital synchronous circuit using multiphase clock signals.

A conventional digital synchronous circuit is formed by a multiphase clock generating circuit 10 for outputting n clock signals CLK1 to CLKn, latch circuits 20 and 30 each of n bits, a clock phase determination circuit 50, a selector 60 for selecting and outputting one clock signal from n clock

signals CLK1 to CLKn.

In addition, latch circuit 20 of n bits is formed by n D-type flip-flops FF1 to FFn.

Now, the connections of the conventional digital synchronous circuit will be described.

Clock signals CLK1, CLK2, . . ., CLKn output from multiphase clock generating circuit 10 are applied respectively to the clock input terminals of flip-flops FF1, FF2, . . ., FFn within latch circuit 20 and respectively to a first data input terminal, a second data input terminal, . . ., and an n-th data input terminal of selector 60. An input data signal DIN is provided to all data input terminals of flip-flops FF1 to FFn.

Moreover, output signals of flip-flops FF1, FF2, . . ., FFn are respectively applied to a first-bit data input terminal, a second-bit data input terminal, . . ., and an n-th bit data input terminal of latch circuit 30 of n bits. A clock input terminal of latch circuit 30 of n bits is provided with a clock signal CLKn.

The output signals of n bits from latch circuit 30 are applied to input terminals of clock phase determination circuit 50.

Further, a clock selecting signal CSL output from clock phase determination circuit 50 is provided to a control input terminal of selector 60, and an output clock signal OUTCLK is output from an output terminal of selector 60.

Now, the operation of the conventional digital synchronous circuit will be described.

Multiphase clock generating circuit 10 outputs clock signals CLK1 to CLKn each having the same frequency as input data signal DIN and each having different phases.

Input data signal DIN is latched by flip-flops FF1, FF2, . . ., FFn within latch circuit 20 respectively according to clock signals CLK1 to CLKn output from multiphase clock generating circuit 10. Thus, input data signal DIN is sampled by clock signals CLK1 to CLKn, and the sampled data is held in flip-flops FF1 to FFn.

The sampled data held in flip-flops FF1 to FFn are taken into latch

circuit 30 forming the next stage by clock signal CLKn.

Then, n bits of data held in latch circuit 30 are provided to clock phase determination circuit 50.

Here, clock phase determination circuit 50 determines the state of the change in the potential level of the signal obtained by sampling input data signal DIN in time sequence to output clock selecting signal CSL for selecting one of clock signals CLK1 to CLKn as the most suitable clock signal for correctly sampling input data DIN.

Selector 60 selects one of clock signals CLK1 to CLKn based on the value of clock selecting signal CSL, and outputs the selected signal as output clock signal OUTCLK.

As described above, one of clock signals CLK1 to CLKn having a phase synchronized with input data signal DIN is selected and the selected signal is output as output clock signal OUTCLK. Thus, a synchronous circuit that operates by digital control is implemented.

Here, the problem of meta-stable phenomenon arises where the outputs of flip-flops FF1 to FFn within latch circuit 20 become temporarily unstable under certain conditions.

The meta-stable phenomenon occurs when the point of change in the potential of input data signal DIN input to flip-flops FF1 to FFn and a point of change in the potential of clock signals CLK1 to CLKn provided to the clock input terminals of flip-flops FF1 to FFn coincide in time.

When the meta-stable phenomenon occurs, the potential of an output of a flip-flop which is the sampling result of input data signal DIN temporarily becomes intermediate, that is, neither at the logic high ("H") level nor at the logic low ("L") level, and thus unstable.

If an output from this flip-flop is taken into latch circuit 30 before the unstable state of the potential settles to either the "H" level or the "L" level, there is a possibility that the potential of an output from latch circuit 30 also becomes intermediate or neither at the "H" level nor at the "L" level due to the meta-stable phenomenon, causing the potential level to be temporarily indefinite.

Thus, the occurrence of the meta-stable phenomenon in flip-flops

FF1 to FFn adversely affects the operation of a circuit that receives the signal having the intermediate potential, thereby making it difficult to output the output clock signal OUTCLK, which is an output of the digital synchronous circuit, in a normal manner.

To avoid such an indefinite state of data, such measures are contemplated as forming latch circuit 30 by flip-flop circuits each having a master-slave construction or connecting such flip-flop circuits in multiple stages to gain enough time for the meta-stable state to be resolved.

Implementing such flip-flop circuits each with a master-slave construction or the multiple-stage connection thereof to gain time, however, increases the circuit scale, creating disadvantages with respect to the chip area and power consumption.

Moreover, when such flip-flop circuits each with a master-slave construction or the multiple-stage connection thereof is implemented, the circuit scale of the corresponding portion would be proportionate to n. Thus, the greater the value of n is, the greater the disadvantages become with respect to the chip area and power consumption.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a digital synchronous circuit which limits the increase in chip size as well as in power consumption and which can avoid the problem of meta-stable phenomenon that occurs when input data signal DIN sent in asynchronous manner is latched by each of a plurality of clock signals CLK1 to CLKn.

In short, the present invention is a digital synchronous circuit provided with a clock generating circuit, a plurality of first latch circuits, a plurality of second latch circuits, and a control circuit. The clock generating circuit outputs a plurality of clock signals. The plurality of first latch circuits are correspondingly provided to the plurality of clock signals, and each of the plurality of first latch circuits receives an input data signal at a data input terminal, and a corresponding clock signal at a clock input terminal. The plurality of second latch circuits are correspondingly provided to the plurality of first latch circuits, and each of the plurality of second latch circuits holds an output signal from a

corresponding one of the plurality of first latch circuits in response to the receipt of a control signal. The control circuit receives the input data signal and generates a control signal. The control circuit outputs the control signal after a delay of a prescribed period of time from the change in the input data signal.

The main advantage of the present invention is that a stable and highly reliable digital synchronous circuit unaffected by the meta-stable state is produced even when there is a first latch circuit among a plurality of first latch circuits that enters into the meta-stable phenomenon due to the point of change in an input data signal coinciding with the point of change in a clock signal. This is made possible by setting the delay of the prescribed period of time longer than the time period required for the meta-stable state to be resolved, since a second latch circuit, which corresponds to the first latch circuit entering into the meta-stable state and which receives an output signal from this first latch circuit, receives a control signal at a clock input terminal after the prescribed period of time from the timing at which the input data signal changes.

In addition, unless the input data signal changes, a control signal would not be output and thus the second latch circuit would not be operated so that the power consumption can be effectively reduced.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of the configuration of a digital synchronous circuit according to a first embodiment or a second embodiment of the present invention.

Fig. 2 is a block diagram of the internal configuration of a latch control circuit 40 of the digital synchronous circuit shown in Fig. 1.

Fig. 3 is a timing chart related to the description of an operation of the digital synchronous circuit when employing latch control circuit 40 shown in Fig. 2.

Fig. 4 is a diagram of the internal configuration of a latch control circuit 40a according to the second embodiment of the present invention in the block configuration of the digital synchronous circuit shown in Fig. 1.

Fig. 5 is a timing chart related to the description of an operation of latch control circuit 40a shown in Fig. 4.

Fig. 6 is a diagram of the internal configuration of another latch control circuit 40b according to the second embodiment of the present invention.

Fig. 7 is a diagram of the internal configuration of yet another latch control circuit 40c according to the second embodiment of the present invention.

Fig. 8 is a block diagram of the configuration of a prior art digital synchronous circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

Fig. 1 is a block diagram of the configuration of a digital synchronous circuit according to a first embodiment of the present invention.

The digital synchronous circuit is formed by a multiphase clock generating circuit 10 for outputting n clock signals CLK1 to CLKn, a latch circuit 20 of n bits for sampling an input data signal DIN, a latch circuit 30 of n bits for latching output signals from latch circuit 20, a latch control circuit 40 for receiving input data signal DIN and generating a signal to be provided to a clock input terminal of latch circuit 30, a clock phase determination circuit 50 for receiving output signals from latch circuit 30 and outputting a clock selecting signal CSL, and a selector 60 for receiving n clock signals CLK1 to CLKn and clock selecting signal CSL and for selecting one of n clock signals CLK1 to CLKn and outputting the selected signal.

In addition, latch circuit 20 of n bits is formed by n D-type flip-flops FF1 to FFn.

The internal configuration of latch control circuit 40 is shown in Fig. 2.

Latch control circuit 40 is formed by a series connection 41 which is

formed by a delay circuit 42 for receiving input data signal DIN and a pulse generating circuit 43 for receiving an output signal from delay circuit 42 and generating a pulse at the point of change in the potential of the output signal.

Pulse generating circuit 43 is formed by an inverter 44 for receiving an output signal from delay circuit 42, an inverter 45 for receiving an input signal from inverter 44, and an exclusive-OR gate 46 (hereinafter referred to as an EXOR gate) for receiving an output signal from delay circuit 42 and an output signal from inverter 45 and outputting a latch control signal LC. Latch control signal LC is an output from pulse generating circuit 43, and thus, from series connection 41.

Now, the connections of the digital synchronous circuit according to the first embodiment will be described.

Referring back to Fig. 1, n clock signals CLK1, CLK2, . . ., CLKn output from multiphase clock generating circuit 10 are applied respectively to the clock input terminals of n flip-flops FF1, FF2, . . ., FFn within latch circuit 20 and respectively to a first data input terminal, a second data input terminal, . . ., and an n-th data input terminal of selector 60.

Input data signal DIN is provided to all data input terminals of flip-flops FF1 to FFn within latch circuit 20 and to an input terminal of delay circuit 42 within latch control circuit 40.

An output terminal of delay circuit 42 is connected to an input terminal of inverter 44 of pulse generating circuit 43 and one input terminal of EXOR gate 46.

An output terminal of inverter 44 is connected to an input terminal of inverter 45, and an output terminal of inverter 45 is connected to the other input terminal of EXOR gate 46.

An output terminal of EXOR gate 46 is connected to a clock input terminal of latch circuit 30 of n bits.

Moreover, output signals of flip-flops FF1, FF2, . . ., FFn are respectively applied to a first-bit data input terminal, a second-bit data input terminal, . . ., and an n-th bit data input terminal of latch circuit 30.

Each of the output signals from a first bit to the n-th bit of latch

circuit 30 is provided to a corresponding input terminal of clock phase determination circuit 50.

In addition, clock phase determination circuit 50 outputs clock selecting signal CSL from an output terminal which is connected to a control input terminal of selector 60. Output clock signal OUTCLK is output from an output terminal of selector 60.

Now, the operation of the digital synchronous circuit according to the first embodiment will be described.

Fig. 3 shows a timing chart of the operation starting from the sampling of input data signal DIN by clock signals CLK1 to CLKn that are multiphase clock signals to the operation of clock phase determination circuit 50.

Multiphase clock generating circuit 10 includes an oscillator, not shown, for generating a signal having the same frequency as input data signal DIN.

Clock signals CLK1 to CLKn that are multiphase clock signals output from multiphase clock generating circuit 10 are of the same frequency, and also coincide with the input data frequency of the input data contained in input data signal DIN.

Moreover, the phases of clock signals CLK1, CLK2, . . ., CLKn are such that the clock signals, in relation to clock signal CLK1, are respectively delayed by 0, $2\pi/n$, $2\pi/n*2$, $2\pi/n*3$, . . ., $2\pi/n*(n-1)$.

Thus, among clock signals CLK1 to CLKn, the clock signals whose clock signal reference numbers are next to one another have a constant phase difference of $2\pi/n$.

Input data signal DIN is latched by flip-flops FF1, FF2, . . ., FFn within latch circuit 20 respectively according to clock signals CLK1 to CLKn output from multiphase clock generating circuit 10.

Here, in Fig. 3, let us assume that the potential of input data signal DIN changes from the "H" level to the "L" level or from the "L" level to the "H" level at time t2.

Further, let us assume that the potential of input data signal DIN is made definite at either the "H" level or the "L" level at time t1 earlier than

time t2 and at time t3 after time t2.

At a timing earlier than time t1 and when the potential of clock signal CLK1 changes from the "L" level to the "H" level, a bit data of input data signal DIN is sampled, and the sampled data is taken into and held by flip-flop FF1 within latch circuit 20.

Then, at a time earlier than time t1 and when enough time has elapsed for the phase of the clock signal to change by $2\pi/n$ after the potential of clock signal CLK1 changes to the "H" level, the potential of clock signal CLK2 changes from the "L" level to the "H" level.

At the time of this change, input data signal DIN is sampled, and the sampled data is taken into and held by flip-flop FF2.

Thereafter, input data signal DIN is sampled in order.

At time t1, the potential of clock signal CLKa changes from the "L" level to the "H" level, and by that time, the potential of input data signal DIN is made definite at either the "H" level or the "L" level so that the definite "H" level or the "L" level is taken into a flip-flop FFa. Here, "a" is 1, an integer satisfying $1<a<n-2$, or n–2.

At time t2 when the phase of the clock signal is delayed by $2\pi/n$ from time t1, the potential of a clock signal CLKa+1 changes from "L" level to the "H" level.

At this time, since it is assumed that the potential of input data signal DIN also changes from the "H" level to the "L" level or from the "L" level to the "H" level, the intermediate potential level amidst the change would be taken in by flip-flop FFa+1.

As a result, flip-flop FFa+1 enters the meta-stable state.

It takes time for the potential of an output of flip-flop FFa+1 to attain the normal state of the "H" level or the "L" level from this meta-stable state.

At time t3 when the phase of the clock signal is delayed by $2\pi/n$ from time t2, the potential of a clock signal CLKa+2 changes from "L" level to the "H" level.

By that time, the potential of input data signal DIN is made definite at either the "H" level or the "L" level so that the definite "H" level or "L" level is taken into a flip-flop FFa+2.

In the similar manner, at a time when enough time has elapsed for the phase of the clock signal to change by $2\pi/n$, input data signal DIN is sampled and the sampled data is held in a corresponding flip-flop within latch circuit 20.

Thus, input data signal DIN is sampled in time sequence by clock signals CLK1, CLK2, . . ., CLKn, and the sampled results are respectively stored flip-flops FF1, FF2, . . ., FFn.

Moreover, input data signal DIN is delayed by delay circuit 42 within latch control circuit 40, and the delayed signal is input to inverter 44 and EXOR gate 46.

At time t4 which is the point of change in the potential level of the delayed signal, i. e., the point of change at the rise or the fall of the delayed signal, a positive differential signal of the delayed signal is output as latch control signal LC from an output terminal of EXOR gate 46.

The pulse width of latch control signal LC is substantially the sum of the delay times of two stages of inverters, that is, the sum of the respective delay times of inverters 44 and inverter 45.

In addition, a delay time d1 from the point of change of input data signal DIN to the outputting of latch control signal LC is the sum of the delay time caused by delay circuit 42 and the delay time caused by EXOR gate 46.

Outputs of flip-flops FF1 to FFn are taken into and held by latch circuit 30 forming the next stage according to latch control signal LC and are held therein.

Now, the contents held in latch circuit 30 will be described.

For instance, let us suppose a case in which the potential of input data signal DIN changing from the "L" level to the "H" level was sampled by clock signals CLK1 to CLKn.

At this time, of the contents held in the first bit to the n-th bit of latch circuit 30, "0" is stored in each of the first bit through a certain bit, and "1" is stored in each of the remaining bits up to the n-th bit.

Thus, the contents starting from the first bit are as follows: "0, 0, ..., 0, 1, 1, ..., 1."

On the other hand, in the case in which the potential of input data signal DIN changes from the "H" level to the "L" level, "1" is stored in each of the first bit through a certain bit, and "0" is stored in each of the remaining bits up to the n-th bit.

Thus, the contents starting from the first bit would be as follows: "1, 1, ..., 1, 0, 0, ..., 0."

Moreover, if no potential change occurs to input data signal DIN, the contents held in the first bit to the n-th bit of latch circuit 30 would be all "0"s or all "1"s.

Further, n bits of data held in latch circuit 30 are provided to clock phase determination circuit 50.

Here, based on n bits of output data from latch circuit 30 that holds signals obtained by sampling input data signal DIN in time sequence, clock phase determination circuit 50 determines the timing for the clock signal most suitable for correctly sampling input data signal DIN.

One of clock signals CLK1 to CLKn is selected as the signal having a timing closest to the determined timing, and a clock selecting signal CSL indicating the value of the clock signal reference number for the selected clock signal is output from clock phase determination circuit 50.

The period between time t2 which is a point of change of input data signal DIN and time t5 which is the next point of change becomes the reception period for each bit data. In order correctly to sample each of the bit data contained in input data signal DIN, the operation margin for sampling the bit data becomes the largest at time ts which is the intermediate timing between time t2 and time t5.

Thus, clock phase determination circuit 50 selects from clock signals CLK1 to CLKn one clock signal whose timing of the rise or the fall is closest to the timing of the middle of each data input serially as input data signal DIN, indicated by time ts.

Specifically, the output data of n bits from latch circuit 30 is checked for a point of change from "0" to "1" in order starting from the first bit. If the point of change is at the b-th bit, clock signal CLKb+n/2 corresponding to the b+n/2 th bit is selected, b+n/2 being the result of adding n/2 to the

value of b.

Otherwise, the point of change from "1" to "0" is checked in order starting from the first bit. If the point of change is at the b-th bit, clock signal CLKb+n/2 corresponding to the b+n/2 th bit is selected, b+n/2 being the result of adding n/2 to the value of b.

A clock selecting signal CSL indicating the value b+n/2 for the clock signal reference number of the selected clock signal CLKb+n/2 is output from clock phase determination circuit 50.

Further, if the value b+n/2 exceeds the value of n, the value of b+n/2–n may be employed.

Next, selector 60 selects one of clock signals CLK1 to CLKn based on the value indicated by clock selecting signal CSL, and outputs the selected signal as output clock signal OUTCLK from an output terminal.

As described above, input data signal DIN and clock signals CLK1 to CLKn are asynchronous so that a flip-flop provided with a clock signal, among clock signals CLK1 to CLKn, whose point of change coincides with the point of change of input data signal DIN enters the meta-stable state, creating a period during which the potential of the output signal of the flip-flop becomes indefinite.

Therefore, the digital synchronous circuit is provided with latch control circuit 40 formed by delay circuit 42, inverters 44 and 45, and EXOR gate 46 so as to delay input data signal DIN by delay circuit 42 within latch control circuit 40 and to generate by inverters 44 and 45 and EXOR gate 46 a latch control signal LC which is a pulse signal at the point of change of the delayed signal.

Further, each of n output signals of latch circuit 20 into which input data signal DIN is sampled in time sequence is latched into latch circuit 30 at the timing of provision of latch control signal LC.

As a result, even when one of flip-flops FF1 to FFn within latch circuit 20 enters the meta-stable state, the timing of generation of latch control signal LC can be delayed until after the time when the normal "H" level or "L" level state is restored from the meta-stable state in order to avoid the adverse influence of the meta-stable state.

Thus, the outputs from flip-flops FF1 to FFn can be latched into latch circuit 30 when the potentials of the outputs are stabilized so that a logic circuit in a stage succeeding latch circuit 30 can be made to operate reliably, effectively allowing a stable operation.

Moreover, since latch control signal LC is generated corresponding to the point of change in input data signal DIN, a logic circuit downstream latch circuit 30 does not operate when no change occurs in the potential level of input data signal DIN. Consequently, unnecessary operation of the digital synchronous circuit is eliminated and power consumption can be effectively limited.

This effect becomes greater when the value of n is larger.

In addition, in the conventional example, to avoid the problem that arises from the fact that the potential of an output of a latch remains indefinite owing to the meta-stable phenomenon, latch circuit 20 is formed as flip-flop circuits each having a master-slave construction or is implemented in the form of such flip-flop circuits connected in multiple stages in order to abide enough time until the meta-stable state is resolved.

According to the present invention described in relation to the first embodiment, when compared with the conventional method, there is no need to employ n flip-flop circuits each having a master-slave construction or to connect the n flip-flop circuits each having a master-slave construction in multiple stages so that a reduction in the circuit scale can be achieved and no increase in the chip area takes place.

Such effects become even greater when the value of n is larger, since only one latch control circuit 40 is required even when the value of n is large.

Moreover, the connections of delay circuit 42 and pulse generating circuit 43 in series connection 41 within latch control circuit 40 shown in Fig. 2 are modified, and input data signal DIN which is an input signal for series connection 41 is provided to an input terminal of inverter 44 which is an input of pulse generating circuit 43 and to one input terminal of EXOR gate 46.

An output terminal of pulse generating circuit 43 may be connected

to an input terminal of delay circuit 42, and latch control signal LC may be output from an output terminal of delay circuit 42. Here, latch control signal LC also becomes an output of series connection 41.

Thus, the same effects as those described in relation to the first embodiment can be achieved with such modifications.

Second Embodiment

The digital synchronous circuit according to the second embodiment employs a latch control circuit 40a obtained by modifying the internal arrangement of latch control circuit 40 of the first embodiment shown in Fig. 2. Other portions are the same as those in the first embodiment.

In other words, the block configuration of the digital synchronous circuit here is the same as that of the first embodiment shown in Fig. 1 so that the descriptions of the connections and the operations of the digital synchronous circuit will not be repeated here except in relation to latch control circuit 40a.

The internal configuration of latch control circuit 40a according to the second embodiment is shown in Fig. 4.

Latch control circuit 40 is formed by a pulse generating circuit 43 for receiving input data signal DIN, a flip-flop 401 for receiving an output signal from pulse generating circuit 43, an N-channel MOS transistor 402 connected to flip-flop 401, a level determination circuit 410 for receiving an output signal and an inverted output signal from flip-flop 401, and a pulse generating circuit 420 for receiving an output signal from level determination circuit 410.

Pulse generating circuit 43 is formed by inverters 44 and 45, and EXOR gate 46.

Level determination circuit 410 is formed by a comparator 411 for comparing an output signal from flip-flop 401 with a reference potential Vref, a comparator 412 for comparing an inverted output signal from flip-flop 401 with reference potential Vref, and an NAND gate 413 for receiving output signals from comparators 411 and 412.

Pulse generating circuit 420 is formed by inverter 421 and an NOR gate 422.

Now, in the digital synchronous circuit according to the second embodiment, the connections of latch control circuit 40a, shown in Fig. 4, which is the modified part from the first embodiment, will be described.

Input data signal DIN is provided to an input terminal of inverter 44 and to one input terminal of EXOR gate 46 within pulse generating circuit 43, and an output terminal of inverter 44 is connected to an input terminal of inverter 45.

An output terminal of EXOR gate 46 is connected to a data input terminal and a clock input terminal of flip-flop 401 and to a gate electrode of N-channel MOS transistor 402.

An output terminal Q of flip-flop 401 is connected to one of the source/drain electrodes of N-channel MOS transistor 402 and to a – input terminal of comparator 411 within level determination circuit 410.

An inverted output terminal QB of flip-flop 401 is connected to the other of the source/drain electrodes of N-channel MOS transistor 402 and to a – input terminal of comparator 412 within level determination circuit 410.

Reference potential Vref is provided to + input terminals of comparators 411 and 412.

In addition, output terminals of comparators 411 and 412 are respectively connected to one and the other input terminals of NAND gate 413.

An output terminal of NAND gate 413 is connected to an input terminal of inverter 421 and one input terminal of NOR gate 422 within pulse generating circuit 420. An output terminal of inverter 421 is connected to the other input terminal of NOR gate 422.

Latch control signal LC is output from an output terminal of NOR gate 422.

Now, the operation of the digital synchronous circuit according to the second embodiment will be described.

Here, since latch control signal LC from input data signal DIN in latch control circuit 40a is generated in a manner different from that in the first embodiment, the operation for generating latch control signal LC will be described. The operations of other portions are the same as those in the

first embodiment so that the descriptions thereof will not be repeated.

Fig. 5 shows a timing chart related to the generation of latch control signal LC by latch control circuit 40a shown in Fig. 4.

At time t20, at either of the points of change upon the rise and upon the fall of input data signal DIN, a positive pulse is generated by pulse generating circuit 43 within latch control circuit 40. This positive pulse is applied to the data input terminal and the clock input terminal of flip-flop 401 at the same time.

As a result, although flip-flop 401 attempts to take in the signal provided to the data input terminal at the timing when the potential of the signal provided to the clock input terminal changes from the "L" level to the "H" level, the signal provided to the data input terminal also is changing from the "L" level to the "H" level so that an intermediate potential that is neither at the "L" level or the "H" level would be taken in, causing flip-flop 401 to enter the meta-stable state.

At the same time, this positive pulse is applied to a gate electrode of N-channel MOS transistor 402, and thus N-channel MOS transistor 402 is rendered conductive so that output terminal Q and inverted output terminal QB of flip-flop 401 are connected, making the meta-stable state more definite. In the meta-stable state, the potentials of output terminal Q and inverted output terminal QB of flip-flop 401 are both neither at the "L" level or the "H" level but are respectively at an intermediate potential.

The intermediate potential state is unstable, and the potentials of output terminal Q and inverted output terminal QB of flip-flop 401 attain either the "L" level or the "H" level after a certain period of time.

Level determination circuit 410 is provided to detect when an output of flip-flop 401 attains either the "L" level or the "H" level from the meta-stable state.

Comparators 411 and 412 are provided within level determination circuit 410 to compare the respective potentials of an output signal and an inverted output signal from flip-flop 401 with the potential of a signal line to which a reference voltage Vref is provided.

For instance, the timing chart of Fig. 5 shows the case in which the

potential of an output signal from flip-flop 401 becomes approximately 1/2 Vdd as soon as the meta-stable state occurs, and attains the "H" level after a certain period of time. Here, Vdd is a power-supply potential.

The value of reference voltage Vref satisfies 1/2 Vdd < Vref < Vdd. In practice, reference voltage Vref of a value close to the potential of Vdd is provided.

The potential of an output signal from flip-flop 401 becomes approximately 1/2 Vdd as soon as the meta-stable state occurs, and assuming that, at time t21, the potential of the output signal from flip-flop 401 becomes higher than the potential of the signal line to which reference voltage Vref is provided, the potential of an output from comparator 411 within level determination circuit 410 attains the "L" level as soon as the meta-stable state occurs at time t20, and then, at time t21 the output from comparator 411 is inverted and attains the "H" level.

On the other hand, the potential of an inverted output signal from flip-flop 401 becomes approximately 1/2 Vdd as soon as the meta-stable state occurs, and attains the "L" level after a certain period of time.

As a result, between time t20 and time t21 and after time t21, the potential of the inverted output signal from flip-flop 401 provided to the – input terminal of comparator 412 within level determination circuit 410 is lower than the potential of the signal line to which reference voltage Vref is provided so that the potential of the output from comparator 412 is at the "H" level.

Consequently, an inverted signal of the output signal from comparator 411 is output from an output terminal of NAND gate 413 that receives output signals respectively from comparators 411 and 412. Thus, at time t21, the potential of an output from NAND gate 413 changes from the "H" level to the "L" level.

Pulse generating circuit 420 that receives the output signal from NAND gate 413 outputs a positive pulse according to the fall of the output signal from NAND gate 413, and the pulse signal becomes latch control signal LC.

Thus configured, latch control circuit 40a according to the second

embodiment forces flip-flop 401 to enter the meta-stable state at the point of change in input data signal DIN, and outputs latch control signal LC at the delayed timing after enough time has elapsed for the meta-stable state of flip-flop 401 to be resolved.

Thus, according to the second embodiment, a delay time d2 from the point of change in input data signal DIN to the time when latch control signal LC is output is the sum of the respective delay times of pulse generating circuit 43, flip-flop 401, level determination circuit 410, and pulse generating circuit 420, but the most dominant delay time is the time period from the occurrence to the resolution of the meta-stable state effected by flip-flop 401 and level determination circuit 410.

Moreover, another latch control circuit 40b shown in Fig. 6 may be employed in place of latch control circuit 40a shown in Fig. 4.

In latch control circuit 40b shown in Fig. 6, comparators 411 and 412 within level determination circuit 410 and the signal line to which a reference voltage Vref is provided are eliminated from latch control circuit 40a shown in Fig. 4, and inverters 414 and 415 are provided in place of comparators 411 and 412, respectively.

An input terminal of inverter 414 is connected to output terminal Q of flip-flop 401 and to one of source/drain electrodes of N-channel MOS transistor 402, and an input terminal of inverter 415 is connected to inverted output terminal QB of flip-flop 401 and to the other of source/drain electrodes of N-channel MOS transistor 402.

In addition, output terminals of inverters 414 and 415 are respectively connected to one and the other of input terminals of NAND gate 413.

The connections of other portions are the same as in latch control circuit 40a shown in Fig. 4 so that the descriptions thereof will not be repeated here.

The operation using another latch control circuit 40b shown in Fig. 6 will be described below.

The values of logical threshold voltages of the respective inverters 414 and 415 within level determination circuit 410 exceed 1/2 Vdd, and

thus are set at a sufficiently high level. The logical threshold voltages of inverters 414 and 415 correspond to reference voltage Vref provided to comparators 411 and 412 shown in Fig. 4.

Inverters 414 and 415 detect the timing at which an output from flip-flop 401 attains the potential of the "L" level or the "H" level from the meta-stable state. Thus, inverters 414 and 415 are made to perform the same function as comparators 411 and 412 shown in Fig. 4.

The operations of latch control circuit 40b other than the above-described operation are the same as those of latch control circuit 40a shown in Fig. 4 so that the descriptions thereof will not be repeated.

Moreover, yet another latch control circuit 40c shown in Fig. 7 may be employed in place of latch control circuit 40a shown in Fig. 4 or of latch control circuit 40b shown in Fig. 6.

The connections of latch control circuit 40c shown in Fig. 7 are formed by changing the connections of flip-flop 401 and comparators 411 and 412 in latch control circuit 40a shown in Fig. 4.

Thus, an output terminal Q of flip-flop 401 is connected to a – input terminal of comparator 411, to a + input terminal of comparator 412 within level determination circuit 410, and to one of source/drain electrodes of an N-channel MOS transistor 402.

An inverted output terminal QB of flip-flop 401 is connected to the other of the source/drain electrodes of N-channel MOS transistor 402.

A reference voltage Vref + is provided to a + input terminal of comparator 411, and a reference voltage Vref – is provided to a – input terminal of comparator 412.

The connections of other portions of latch control circuit 40c shown in Fig. 7 are the same as in latch control circuit 40a shown in Fig. 4 so that the descriptions thereof will not be repeated.

Now, the operation using latch control circuit 40c shown in Fig. 7 will be described below.

The value of reference voltage Vref + satisfies 1/2 Vdd < Vref + <Vdd. In practice, reference voltage Vref + of a value close to the potential of Vdd is provided. In addition, the value of reference voltage Vref – satisfies 0 <

Vref < 1/2 Vdd. In practice, reference voltage Vref – of a value close to the ground potential is provided.

Flip-flop 401 enters the meta-stable state, and the potential of an output signal from flip-flop 401 becomes approximately 1/2 Vdd. After a certain period of time, the potential attains the "H" level or the "L" level.

When the potential of an output from flip-flop 401 attains the "H" level from approximately 1/2 Vdd, comparator 411 detects the timing at which the "H" level is attained. When the potential of an output attains the "L" level from approximately 1/2 Vdd, comparator 412 detects the timing at which the "L" level is attained.

Other operations are the same as those of latch control circuit 40a shown in Fig. 4, and the descriptions thereof will not be repeated here.

As described above, the digital synchronous circuit is provided with flip-flop 401 for causing the meta-stable state in latch control circuit 40a shown in Fig. 4, another latch control circuit 40b shown in Fig. 6 or yet another latch control circuit 40c shown in Fig. 7, and comparators 411 and 412 or inverters 414 and 415 for determining whether the meta-stable state is resolved. In this case, if flip-flop 401 is formed of the same circuit as the flip-flop employed for flip-flops FF1 to FFn within latch circuit 20, even when one of flip-flops FF1 to FFn enters the meta-stable state, latch control signal LC would be output at the timing that corresponds to the time required for the resolution of the meta-stable state of the flip-flop that entered the meta-stable state.

As a result, at the time output signals from flip-flops FF1 to FFn are latched into latch circuit 30, and thus, at the time latch control circuit LC is output, the potential of the data input terminal of latch circuit 30 is not at an intermediate potential but at the "H" level or the "L" level.

Thus, latch circuit 30 never enters the meta-stable state, and therefore the digital synchronous circuit can be operated with reliability.

Moreover, even when the time required for the meta-stable state in flip-flops FF1 to FFn to be resolved varies due to temperature variation, voltage variation, and manufacturing process, the same variation would be applied to the timing of outputting of latch control signal LC so that the

digital synchronous circuit can be operated with reliability.

Furthermore, latch circuit 30 is operated after it is delayed only for the actual time period in which the meta-stable state is taking place. In comparison with the case where the worst possible value for the meta-stable time that varies due to temperature variation, voltage variation, and manufacturing process is estimated at the designing stage, and where latch control signal LC is output after the delay of the fixed time period corresponding to the worst possible value of the meta-stable time from the point of change in input data signal DIN, latch control signal LC is not delayed any longer than is necessary so that the timing at which output signals from latch circuit 20 are latched by latch circuit 30 can be made earlier.

Thus, delay time d2 for latch control circuits 40a to 40c according to the second embodiment is shorter than delay time d1 for latch control circuit 40 according to the first embodiment.

In addition, the internal configuration of latch control circuit 40a shown in Fig. 4 or of another latch control circuit 40b shown in Fig. 6 may be partially modified.

More specifically, in latch control circuit 40a shown in Fig. 4 or in another latch control circuit 40b shown in Fig. 6, NAND gate 413 within level determination circuit 410 and pulse generating circuit 420 may be eliminated, and a 2-input NOR gate and another pulse generating circuit may be added in place of NAND gate 413 and pulse generating circuit 420, respectively.

This additional pulse generating circuit is formed to output a positive pulse signal at the rise of the signal that is input into it.

In addition to the above, in the case that the internal configuration of latch control circuit 40a shown in Fig. 4 is partially modified, a positive voltage close to a ground potential may be applied as a reference voltage Vref, whereby the same operation and the same effects are allowed as latch control circuit 40a shown in Fig. 4 of the second embodiment.

Further, in the case that the internal configuration of another latch control circuit 40b shown in Fig. 6 is partially modified, the values of logical

threshold voltages of inverters 414 and 415 may be further changed so that the values are set to be not higher than 1/2 Vdd and as close as possible to a ground potential, thereby achieving the same operation and the same effects as latch control circuit 40b shown in Fig. 6 of the second embodiment.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A digital synchronous circuit, comprising:

a clock generating circuit for outputting a plurality of clock signals having same frequency and different phases;

a plurality of first latch circuits for taking in an input data signal according to corresponding ones of said plurality of clock signals;

a control circuit for outputting a control signal after a prescribed period of time according to a change in said input data signal; and

a plurality of second latch circuits for taking in and holding outputs of said plurality of first latch circuits, respectively, according to said control signal.

2. The digital synchronous circuit according to claim 1, further comprising:

a clock phase determination circuit for monitoring data held in said plurality of second latch circuits to determine an internal clock signal matching in phase with said input data signal from said plurality of clock signals; and

a selector for selecting an internal latch clock signal for suitably sampling said input data signal from said plurality of clock signals according to an output from said clock phase determination circuit and outputting selected said internal latch clock signal.

3. The digital synchronous circuit according to claim 2, wherein said control circuit includes

a delay circuit for receiving said input data signal to cause delay for said prescribed period of time, and

a pulse generating circuit for generating a pulse signal according to a change in output from said delay circuit.

4. The digital synchronous circuit according to claim 2, wherein said control circuit includes

a pulse generating circuit for generating a pulse signal according to a change in said input data signal, and

a delay circuit for receiving said pulse signal to cause delay for said prescribed period of time.

5. The digital synchronous circuit according to claim 2, wherein said control circuit includes

a first pulse generating circuit for generating a first pulse signal according to a change in said input data signal,

a third latch circuit for receiving said first pulse signal at a data input node and a clock input node,

a level determination circuit for outputting a detection signal when potential of an output signal from said third latch circuit has crossed a reference potential, and

a second pulse generating circuit for generating a second pulse signal according to a change in potential of said detection signal and outputting said second pulse signal as said control signal.

6. The digital synchronous circuit according to claim 5, wherein said third latch circuit has same circuit configuration as said first latch circuit.

7. The digital synchronous circuit according to claim 5, wherein

said third latch circuit has a first output node for outputting a signal of an equal polarity to said data input signal and a second output node for outputting an inverted output of said signal output from said first output node, and

said control circuit further includes a field-effect transistor connected between said first output node and said second output node for receiving said first pulse signal at a gate.

8. The digital synchronous circuit according to claim 5, wherein said third latch circuit has a first output node for outputting a signal

of an equal polarity to said data input signal and a second output node for outputting an inverted output of said signal output from said first output node, and wherein

said level determination circuit includes

a first level determination unit for determining whether potential of said first output node has reached a prescribed potential level,

a second level determination unit for determining whether potential of said second output node has reached said prescribed potential level, and

a first logic gate circuit for outputting said detection signal according to outputs from said first and second level determination units.

9. The digital synchronous circuit according to claim 8, wherein said first level determination unit includes a first differential input comparator for receiving a potential level of said first output node and said prescribed potential level, and

said second level determination unit includes a second differential input comparator for receiving a potential level of said second output node and said prescribed potential level.

10. The digital synchronous circuit according to claim 8, wherein said first and second level determination units have second and third logic gate circuits, respectively, whose threshold voltages each is said prescribed potential level.

11. The digital synchronous circuit according to claim 5, wherein said level determination circuit includes

a first level determination unit for determining whether potential of an output signal from said third latch circuit has crossed a first potential level,

a second level determination unit for determining whether potential

of an output signal from said third latch circuit has crossed a second potential level lower than said first potential level, and

a first logic gate circuit for outputting said detection signal according to outputs from said first and second level determination units.

12. The digital synchronous circuit according to claim 11, wherein said first level determination unit includes a first differential input comparator for receiving a potential level of an output node of said third latch circuit and said first potential level, and

said second level determination unit includes a second differential input comparator for receiving the potential level of said output node and said second potential level.

13. The digital synchronous circuit according to claim 11, wherein

said first level determination unit includes a second logic gate circuit whose threshold voltage is said first potential level,

said second level determination unit includes a third logic gate circuit whose threshold voltage is said second potential level,

said first potential level is an intermediate potential between a potential that is a half of a power-supply potential and said power-supply potential, and

said second potential level is an intermediate potential between the potential that is a half of said power-supply potential and a ground potential.

ABSTRACT OF THE DISCLOSURE

The present digital synchronous circuit includes a clock generating circuit for outputting a plurality of clock signals CLK1 to CLKn, a plurality of first latch circuits, each for receiving an input data signal DIN at a data input terminal and for receiving a corresponding clock signal at a clock input terminal, a plurality of second latch circuits, each for latching, in response to the receipt of a control signal LC, an output signal from a corresponding first latch circuit, and a control circuit for receiving input data signal DIN to generate control signal LC. Control circuit outputs control signal LC after a delay of a prescribed period of time after the change in input data signal DIN. As a result, the adverse influence of the meta-stable state that occurs when sampling an asynchronous input data signal DIN is avoided, while at the same time, the chip size and power consumption are limited.

FIG. 1

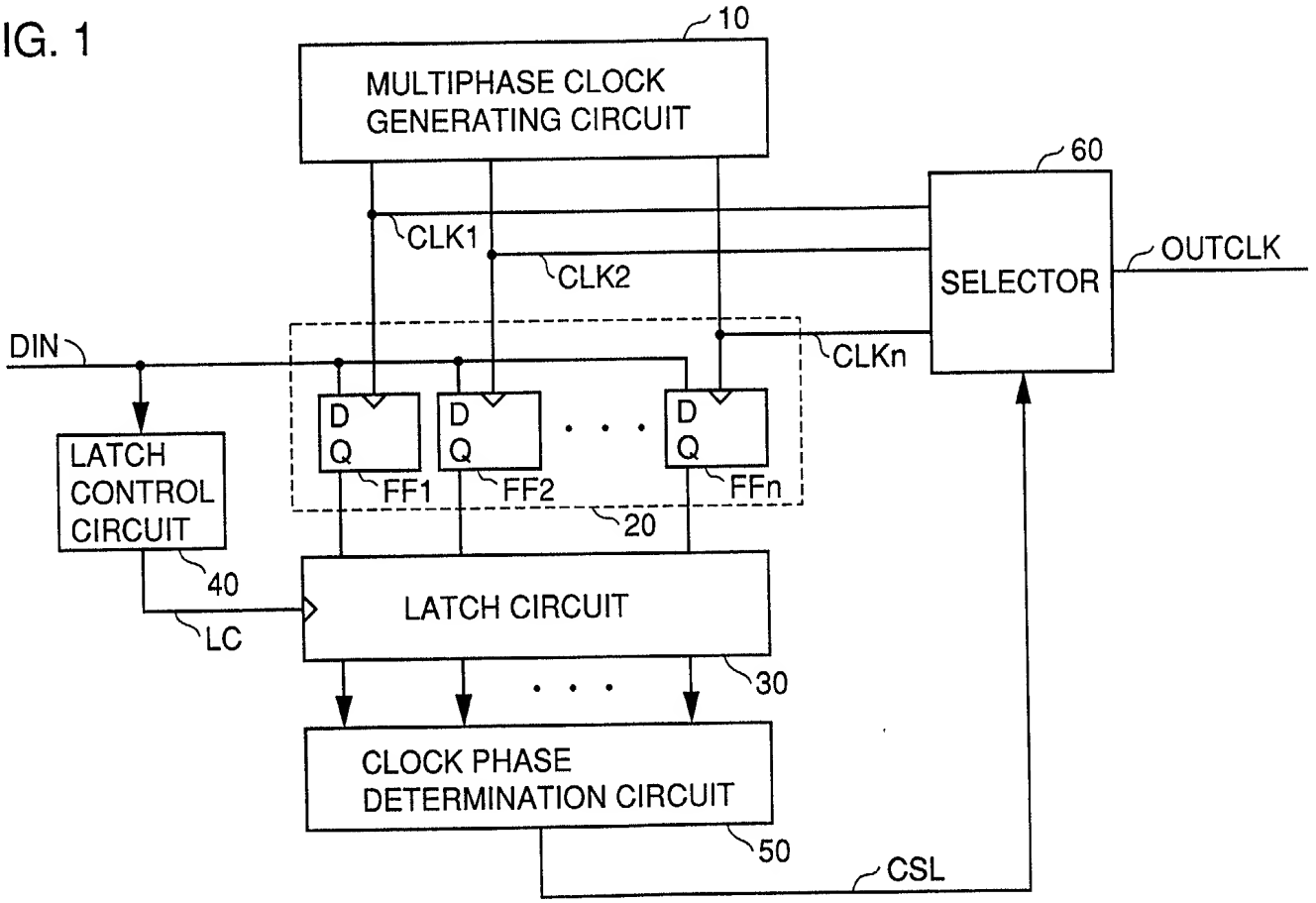


FIG. 2

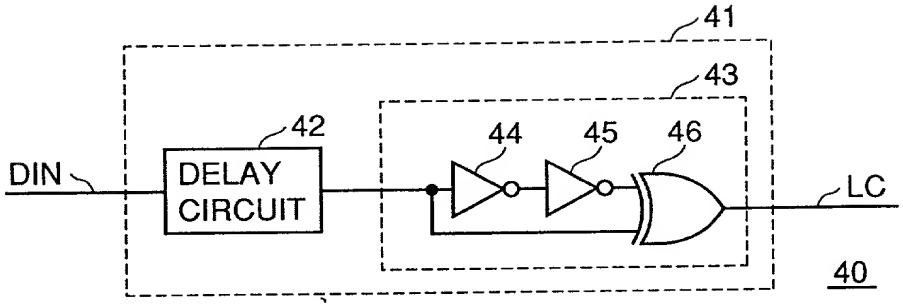


FIG. 3

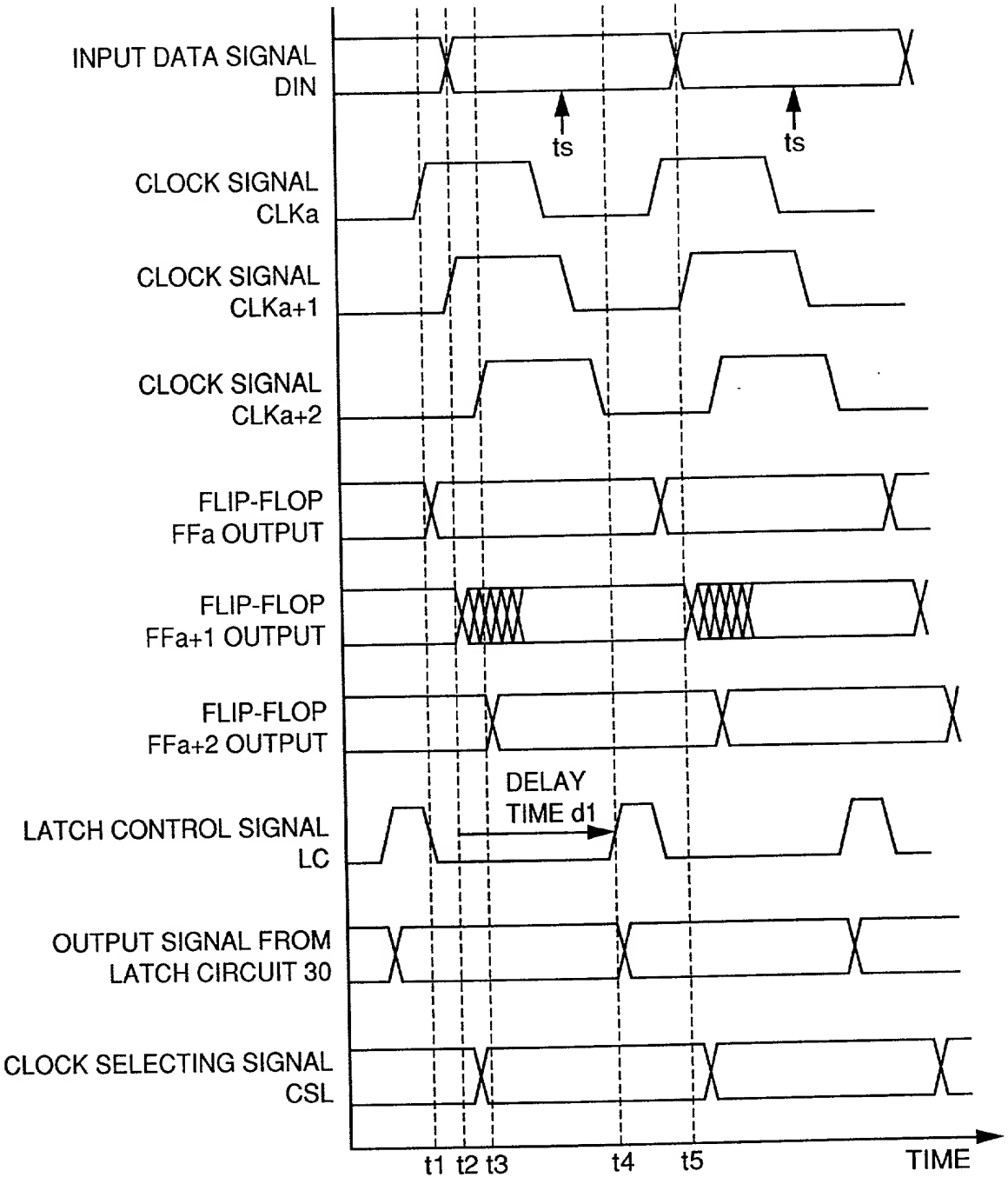

INPUT DATA SIGNAL
DIN
ts
ts
CLOCK SIGNAL
CLKa
CLOCK SIGNAL
CLKa+1
CLOCK SIGNAL
CLKa+2
FLIP-FLOP
FFa OUTPUT
FLIP-FLOP
FFa+1 OUTPUT
FLIP-FLOP
FFa+2 OUTPUT
DELAY
TIME d1
LATCH CONTROL SIGNAL
LC
OUTPUT SIGNAL FROM
LATCH CIRCUIT 30
CLOCK SELECTING SIGNAL
CSL
t1 t2 t3 t4 t5
TIME

FIG. 4

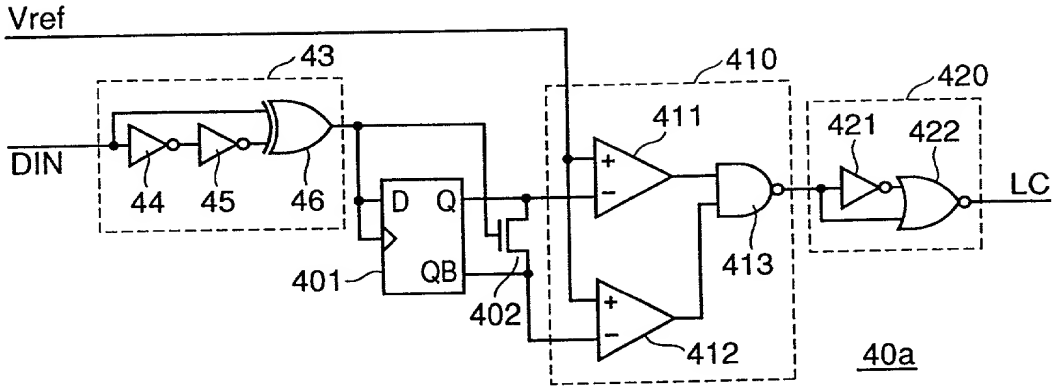

Vref
43
410
420
411
421
422
DIN
44
45
46
D
Q
QB
401
402
413
LC
412
40a

FIG. 5

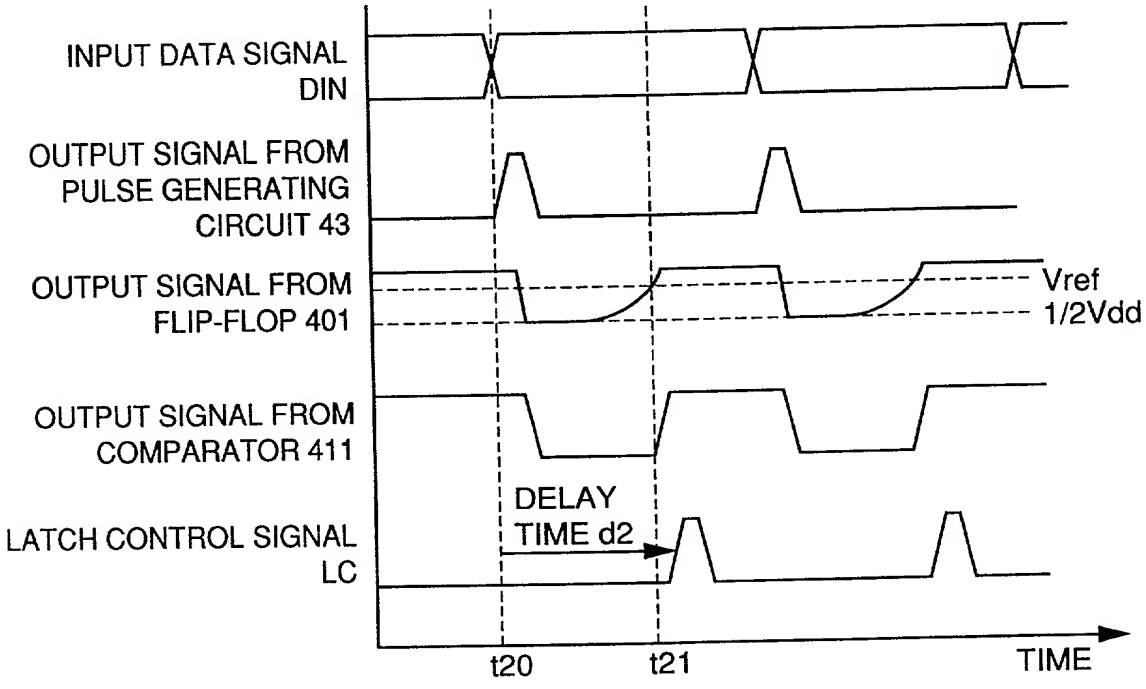

INPUT DATA SIGNAL
DIN
OUTPUT SIGNAL FROM
PULSE GENERATING
CIRCUIT 43
OUTPUT SIGNAL FROM
FLIP-FLOP 401
Vref
1/2Vdd
OUTPUT SIGNAL FROM
COMPARATOR 411
DELAY
TIME d2
LATCH CONTROL SIGNAL
LC
t20
t21
TIME

FIG. 6

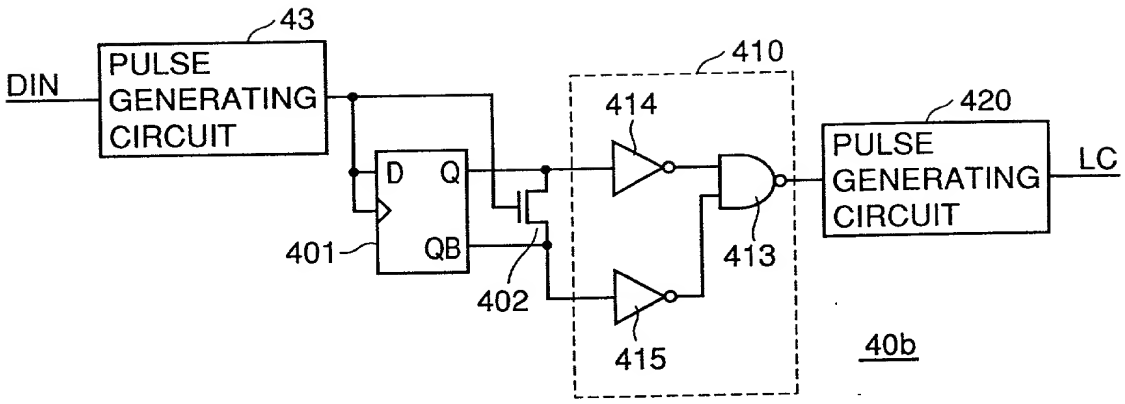

43
DIN
PULSE GENERATING CIRCUIT
D
Q
QB
401
402
410
414
413
415
420
PULSE GENERATING CIRCUIT
LC
40b

FIG. 7

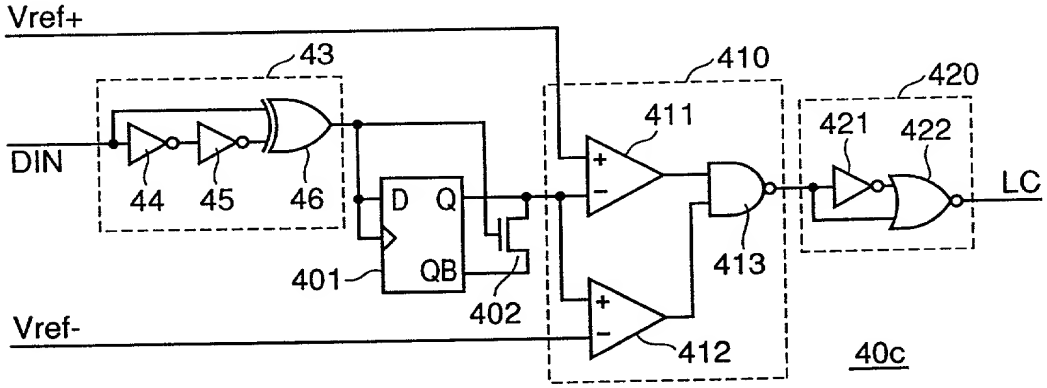
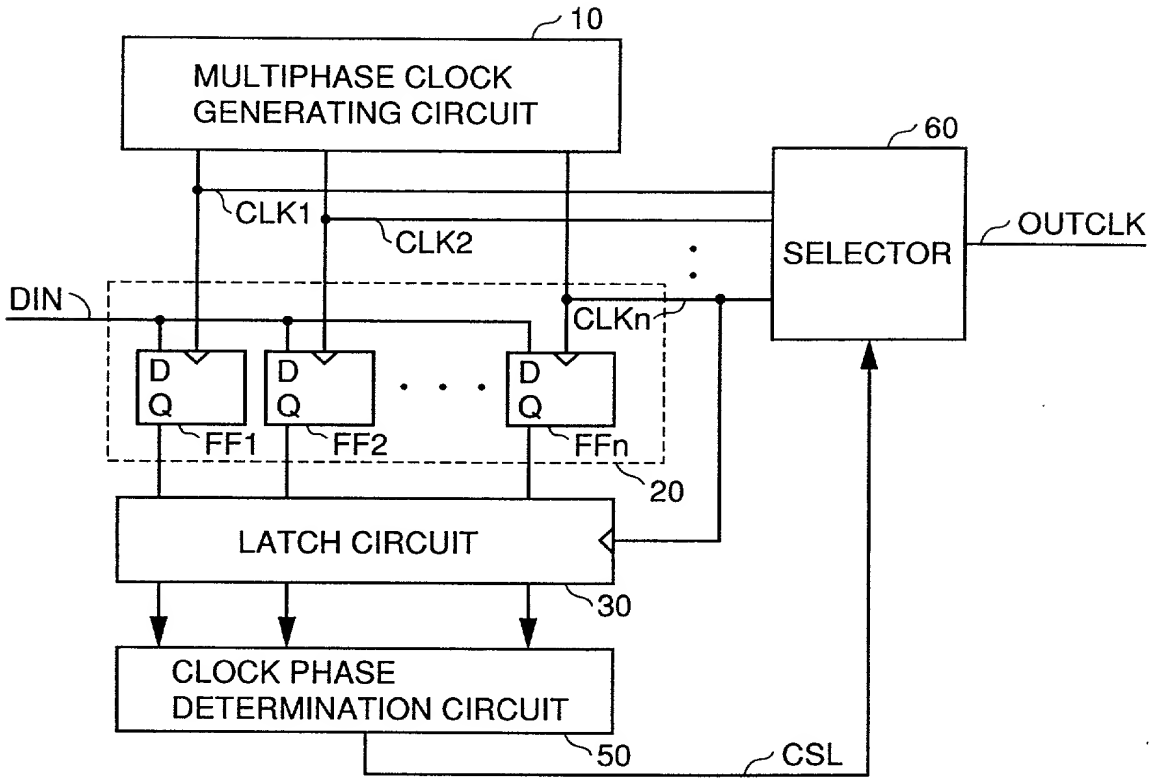

Vref+
43
DIN
44
45
46
D
Q
QB
401
402
Vref-
410
411
412
413
420
421
422
LC
40c

FIG. 8 PRIOR ART



Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名か下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A DIGITAL SYNCHRONOUS CIRCUIT FOR STABLY GENERATING OUTPUT CLOCK SYNCHRONIZED WITH INPUT DATA

その明細書を
（該当する方に印を付す）

the specification of which

(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ _____ 日に出願番号

第 _____ 号として提出し、

_____ 日に補正した。
（該当する場合）

☐ was filed on _____ as

Application Serial No. _____

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第１章第56条（ａ）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

(Number) (番 号)	(Country) (国 名)	(Day/Month/Year Filed) (出願の年月日)	Priority claimed 優先権の主張 Yes あり	No なし
11-347448(P)	Japan	7/December/1999	[X]	[ ]
			[ ]	[ ]
			[ ]	[ ]

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第１項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第１章第56条（ａ）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現 況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。
（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

Stanislaus Aksman, Reg. No. 28,562; Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; William H. Beha, Reg. No. 38,038; John G. Bisbikis, Reg. No. 37,095; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Wilhelm F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Thomas A. Jolly, Reg. No. 39,241; Eric J. Kraus, Reg. No. 36,190; Edward E. Kubasiewicz, Reg. No. 30,020; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael E. McCabe, Jr., Reg. No. 37,182; James H. Meadows, Reg. No. 33,965; Michael A. Messina, Reg. No. 33,424; Joseph H. Paquin, Jr., Reg. No. 31,647; Craig L. Plastrik, Reg. No. 41,254; Robert L. Price, Reg. No. 22,685; Paul A. Roberts, Reg. No. 40,289; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Michele M. Schafer, Reg. No. 34,717; David J. Serbin, Reg. No. 30,589; Glenn Snyder, Reg. No. 41,428; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Leon R. Turkevich, Reg. No. 34,035; Christopher D. Ward, Reg. No. 41,367; Damian G. Wasserbauer, Reg. No. 34,749; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976

書類の送付先：

Send Correspondence to:

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, D.C. 20005-3096

直通電話連絡先：（名称および電話番号）

Direct Telephone Calls to: (*name and telephone number*)

Stephen A. Becker
(202)756-8000

唯一のまたは第一の発明者の氏名	Full name of sole or first inventor Tsutomu YOSHIMURA
同発明者の署名　日付	Inventor's signature　Date Tsutomu Yoshimura　May 15, 2000
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 JAPAN
第２の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any Harufusa KONDOH
同第２発明者の署名　日付	Second inventor's signature　Date Harufusa Kondoh　May 15, 2000
住所	Residence Hyogo, Japan
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha
	2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 JAPAN

（第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)